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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/623,666	07/21/2003	Claes Bjorkman	7090/P2 & 107262.202US1	5063

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EXAMINER	
SONG, SARAH U	
ART UNIT	**PAPER NUMBER**
2874	

DATE MAILED: 04/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/623,666	BJORKMAN ET AL.	
	Examiner	Art Unit	
	Sarah Song	2874	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8-10 and 17-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-10 and 17-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 February 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *0204,1204*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 1-10 in the reply filed on January 31, 2005 is acknowledged. Claims 1-6 and 8-10 have been amended. Claims 7 and 11-16 have been canceled. Claims 17-28 have been added. Claims 1-6, 8-10 and 17-28 are pending.

Information Disclosure Statement

2. The prior art documents submitted by the applicant in the Information Disclosure Statements filed on February 9, 2004 and December 16, 2004 have all been considered and made of record (note the attached copy of form PTO-1449). It is noted that US2004/0012401 is a publication of King et al. not West et al.

Drawings

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: 101 and 103. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

4. Furthermore, Examiner believes that the labeling of layer 14 as "S_2O_2" should be corrected to read "SiO_2".

Specification

5. The disclosure is objected to because of the following informalities: Examiner suggests changing "an oxide of a silicon oxide" to either –an oxide of silicon—or –a silicon oxide—. See page 2, line 26 for example. Appropriate correction is required.

Claim Objections

6. Claim 1 is objected to because of the following informalities: in line 8, Examiner suggests changing "circuit" to –circuitry—. Appropriate correction is required.

7. Claim 3 is objected to because of the following informalities: in line 2, Examiner suggests changing "and" to –an—. Appropriate correction is required.

8. Claim 6 is objected to because of the following informalities: Examiner suggests changing "an oxide of a silicon oxide" to either –an oxide of silicon—or –a silicon oxide—. Appropriate correction is required.

9. Claim 23 is objected to because of the following informalities: the claim depends on a canceled claim; "the topside" and "the first semiconductor chip" lack proper antecedent basis. It appears that claim 23 should depend from claim 1 and will be examined accordingly.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. **Claims 1-6, 8-10 and 17-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Delwala (U.S. Patent 6,658,173) in view of Johnson et al. (U.S. Patent Application Publication 2002/0181825) and Nakamura (U.S. Patent 6,449,411).**

12. Regarding claim 1, Delwala discloses an article of manufacture comprising an optical ready substrate 152 made of a first semiconductor layer 102, an insulating layer 104 on top of the first semiconductor layer, and a second semiconductor layer 160 on top of the insulating layer, wherein the second semiconductor layer has a top surface and is laterally divided into two regions including a first region and a second region (see Figure 1), the top surface of the first region being of a quality that is sufficient to permit microelectronic circuitry to be formed therein (see paragraph spanning columns 12 and 13) and said second region including an optical signal distribution circuit formed therein, said optical signal distribution circuit made up of semiconductor photonic elements (i.e. waveguide devices) interconnected by an optical waveguide (e.g. 161).

13. Delwala does not expressly disclose said optical signal distribution circuit to be designed to provide signals to the microelectronic circuit to be fabricated in the first region of the second semiconductor layer.

14. Johnson et al. discloses an article of manufacture comprising an optical substrate made of semiconductor layers and comprising a first region and a second regions, wherein the first region being of a quality sufficient to permit microelectronic circuitry 3813 to be formed therein and said second region including an optical signal distribution circuit formed therein, said optical signal distribution circuit made up of interconnected semiconductor photonic elements 3815 and

designed to provide signals to the microelectronic circuit 3813 to be fabricated in the first region (see Paragraph [0139]).

15. Delwala and Johnson et al. are analogous art as pertaining to hybrid integrated circuits.

16. It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the optical signal distribution circuit of Delwala such that it was designed to provide signals to the microelectronic circuit to be fabricated in the first region of the second semiconductor layer, as shown by Johnson et al.

17. One of ordinary skill in the art would have been motivated to design the optical distribution circuit of Delwala such that it was designed to provide signals to the microelectronic circuit in the first region in order to provide high speed on-chip communications as taught by Johnson et al. (Paragraph [0141]).

18. Additionally, Delwala does not expressly disclose the waveguide for carrying an optical signal characterized by a wavelength of about 850 nanometers or less. However, it is noted that the functional recitation that the waveguide is for carrying an optical signal characterized by a wavelength of about 850 nm or less has not been given patentable weight because it is narrative in form.

19. Nevertheless, Nakamura discloses planar waveguides which comprise a germanium doped silica core and a silica cladding formed on a silicon substrate (column 5, lines 21-28) and which are capable of carrying an optical signal characterized by a wavelength of about 850 nm or less and therefore meets the claimed limitation.

20. Nakamura is analogous art as pertaining to planar lightwave circuits.

21. It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide silica based waveguide, which is capable of carrying an optical signal characterized by a wavelength of 850 nm or less, since Nakamura discloses that the silica based waveguides provide ease of integration (column 3, lines 34-39).

22. Regarding claim 17, the second semiconductor layer 160 comprises silicon.

23. Regarding claim 23, the topside (top surface) of the semiconductor chip (substrate) comprises silicon (Figures 3-4 of Delwala).

24. Regarding claims 18-22 and 24-28, as noted above, the waveguide includes a core material of silica doped with GeO_2, and a silica cladding.

25. Regarding claims 2-4, resultantly, the semiconductor photonic elements of the optical signal distribution circuit include an output elements couple to the optical waveguide for delivering signals carried by the waveguides to the microelectronic circuitry; the output element is an optical detector which converts optical signals to electrical signals; and the optical signal distribution network is an optical clock signal distribution network (Paragraphs [0138]-[0139]).

26. Regarding claim 5, the first semiconductor layer 102 comprises silicon.

27. Regarding claim 6, the insulating layer 104 comprises an oxide of silicon.

28. Regarding claim 8, the combination of the first semiconductor layer, the insulating layer and the second semiconductor layer is an SOI structure 152.

29. Regarding claim 9, Delwala does not expressly disclose the second region of the second semiconductor layer to be thicker than the first region of the second semiconductor layer. However, it is known in the art to adjust the thickness of layers of an optical circuit in order to optimize waveguiding properties. Therefore, it would have been obvious to one having ordinary

skill in the art to provide the second region of the second semiconductor layer thicker than the first region in order to ensure optimal mode confinement to the waveguides. Furthermore, it is noted that since applicant has not disclosed that the feature solves any stated problem or is for any particular purpose and it appears that the invention would perform equally well with a thicker second region.

30. Regarding claim 10, the top surface of the first region is of a quality that is sufficient to permit CMOS circuitry to be formed therein (see paragraph spanning columns 10 and 11).

Conclusion

31. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sarah Song whose telephone number is 571-272-2359. The examiner can normally be reached on M-Th 7:30am - 6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rodney Bovernick can be reached on 571-272-2344. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sarah Song
Patent Examiner
Group Art Unit 2874